

Conformal Lec User Guide

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~~Introducing Conformal Smart LEC Understanding Logic Equivalence Check in VLSI | What is LEC? S-7 | Logic Equivalence Check using Formality | RTL-to-GDSII flow | Synopsys Formality tutorial~~

Equivalence Checking / Formal Verification **Conformal Mapping Lec 1**
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checking solution. Offering key technologies of massive parallelism and adaptive proof, Conformal Smart LEC improves runtime by an average of 4X compared to existing solutions

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Conformal ECOs at Marvell during pre-mask stage. We have done multiple ECOs using Conformal automated flow on various projects for the past few years. Below is the data for •Example 1 – Block A – Pre-mask ECO was done inside a control block which was instanced multiple(12) times. ECO fix involved combinational logic change in control block.

Practical ECOs using Conformal ECO tool

Conformal Smart Logic Equivalence Checker is the next-generation equivalency checking solution. With massively parallel architecture and adaptive proof technology, the Conformal Smart LEC delivers dramatic turnaround time improvements in equivalence checking by over 20X for RTL-to-gate comparisons.

Conformal Smart LEC - Cadence Design Systems

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Cadence® Conformal® Equivalence Checker (EC) makes it possible to verify and debug multi-million-gate designs without using test vectors. It offers the industry's only complete equivalence checking solution for verifying SoC designs—from RTL to final LVS netlist (SPICE)—as well as FPGA designs.

Conformal Equivalence Checker - Cadence Design Systems

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For the execution of LEC, the Conformal tool requires three types of files. <design_name>.lec file guide the Conformal tool to execute different command in a systematic way. <design_name>.scan_const file provides scan related constraints like if we want to ignore some scan connections/serdes input/output pins which are defined in this file.

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A Guide on Logical Equivalence Checking - Flow, Challenges ...

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